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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/712,229	11/12/2003	Andrew L. Van Brocklin	200309795-1	8482

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EXAMINER	
DHARIA, PRABODH M	
ART UNIT	**PAPER NUMBER**
2629	

SHORTENED STATUTORY PERIOD OF RESPONSE	MAIL DATE	DELIVERY MODE
3 MONTHS	03/26/2007	PAPER

Please find below and/or attached an Office communication concerning this application or proceeding.

If NO period for reply is specified above, the maximum statutory period will apply and will expire 6 MONTHS from the mailing date of this communication.

Office Action Summary	Application No.	Applicant(s)	
	10/712,229	VAN BROCKLIN ET AL.	
	Examiner	Art Unit	
	Prabodh M. Dharia	2629	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *08 February 2007*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-13* is/are pending in the application.

4a) Of the above claim(s) *14-44* is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-13* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *12 November 2003* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

1. **Status:** Please all the replies and correspondence should be addressed to examiner's new art unit 2629. Receipt is acknowledged of papers submitted on 02-08-2007 under amendments, which have been placed of record in the file. Claims 1-13 are pending in this action. Claims 14-44 are withdrawn from consideration.

Response to Amendment

The amendment filed 02-08-2007 does not introduces new matter into the disclosure. The added material which is supported by the original disclosure.

Claim Rejections - 35 USC § 103

2. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

3. Claims 1-3,12,13 are rejected under 35 U.S.C. 103(a) as being unpatentable over Matthies et al. (US 2005/0078104 A1) in view of Hayashi et al. (6,359,666 B1) and Fukuda, Masafumi (US 20020044142 A1).

Regarding Claim 1, Mathis et al. teaches a large area display (page 1, paragraph 2, page 3, paragraph 75, page 4, paragraphs 75,76, 78, 80, page 8, paragraph 116,120, page 9, paragraph 121,122) comprising: a pixel layer including display elements (page 3,4, paragraph 75); a connection layer (page 4, paragraph 76, Lines 1-11 paragraph 78); drivers in communication

with the pixel layer and the connection layer (page 4, paragraph 78), the drivers configured for driving the display elements in the pixel layer and configured for communicating through the connection layer (page 4, paragraph 78, paragraph 80, Lines 1-10); and a laminate formed (page 8, paragraphs 120, Lines 10-13) of the pixel layer, the connection layer and drivers (page 8, paragraphs 116, 120, pages 8,9, paragraph 121) comprising the large area display (page 3, paragraph 71, Lines 1-5). However, Mathis et al. fails to recite or disclose a pixel layer having a repeating pattern of sub-displays formed on a continuous pixel layer sheet, and a connection layer in communication with the drivers having a continuous sheet with conductive traces for distributing power and data to the drivers wherein the pixel layer, the connection layer and the drivers are laminated together to form the large area display. However, Hayashi et al. discloses a pixel layer having a repeating pattern (Col. 1, Lines 49-61, Col. 2, Lines 60-67, Col. 6, Lines 61-67) of sub-displays formed on a continuous pixel layer sheet (Col. 6, Lines 61-67), and a connection layer in communication with the drivers having a continuous sheet (substrate) with conductive traces for distributing power and data to the drivers wherein the pixel layer (Col. 4, Line 55 to Col. 5, Line 2, Col. 6, lines 6-8, Col. 7, Lines 29-37) the connection layer and the drivers are laminated together to form the large area display (see figure 5, Col. 6, Lines 61-67, Col. 5, Lines 3-27, Col. 9, Lines 10-21).

The reason to combine teaching of Hayashi et al. with teaching of Matthis et al. teaching of large area LCD tiled base is Hayashi et al. teaches large LCD display formed with repeating pattern of Pixels, and novel structure of wiring such as signal lines scanning lines and pixel electrodes formed on an array substrate (single sheet).

Thus it is obvious to one in the ordinary skill in the art at the time of invention was made to incorporate teaching of Hayashi et al. in teaching of Matthis et al. to able to have a large area display with active matrix or passive matrix organization, as well as TFT driver for pixels with novel structure of wiring such as signal lines scanning lines and pixel electrodes formed on an array substrate (single sheet) without causing the unevenness of combined images.

Regarding amended Claim1, Mathis et al. fails to address a plurality of drivers, each driver in communication with a corresponding one of the sub-displays and configured for driving the display elements in the sub-display.

However newly cited reference of Fukuda, Masafumi (US 20020044142 A1) discloses plurality of drivers, each driver in communication with a corresponding one of the sub-displays and configured for driving the display elements in the sub-display (see figures 1 and 2 , abstract, page 2, paragraph 21, Lines 21,22, page 6, paragraphs 102-107).

The reason to combine teaching of Fukuda, Masafumi with teaching of Matthis et al. teaching of large area LCD tiled base is Fukuda, Masafumi teaching provides a display driver which, when a display section is driven using a plurality of display drivers can suppress the drop of the power source voltage between respective display drivers thus preventing the deterioration of the display quality of the display section and a display device using such display drivers.

Thus it is obvious to one in the ordinary skill in the art at the time of invention was made to incorporate teaching of Fukuda, Masafumi in teaching of Matthis et al. to able to have a large area display with active matrix or passive matrix organization, as well as TFT driver for pixels and to provide a display driver which, when a display section is driven using a plurality of display drivers can suppress the drop of the power source voltage between respective display

drivers thus preventing the deterioration of the display quality of the display section and a display device using such display drivers and the display driver is constituted such that the operation thereof is changed over between the first mode which generates the driving voltages based on the voltages generated by the voltage generating means and the second mode which generates the driving voltages based on the voltages supplied from the outside. Further, the display driver makes the voltage-follower connected operational amplifier circuit generate the driving voltages. Due to such a constitution, when a display panel having an increased capacity is driven by a plurality of display drivers the display driving can be performed using a plurality of same display drivers so that a manufacturing cost of chips for display drivers suitable for the display driving can be reduced (see pages 1,2 paragraphs 19,20).

Regarding Claim 2, Mathis et al. teaches the drivers are laminated between the pixel layer and the connection layer (item # 510,512,514, 516, 520,522,524, see figure 5, pages 8,9, paragraphs 120,121).

Regarding Claim 3, Mathis et al. teaches the display elements comprises at least one of liquid crystal display (LCD), light emitting diode (LED), organic LED (OLED), polymer light emitting device (PLED), electroluminescent (EL), electrophoretic display, electrochromic display, electrowetting, gas plasma and fiber plasma (page 3, paragraph 70).

Regarding Claim 12, Mathis et al. teaches the drivers further comprise: serial data input for receiving display data (see figures 6,12, page 11, paragraph 140, Lines 13-16 a single line

receiving serial data to each tile of display); and serial data output (page 11, paragraph 139, Lines 11-23, receive pixel data stored in the memory and outputted serially on a single line) for sensing and testing (pages 6, paragraphs 102, 103, page 7, paragraphs 103-108) and the connection layer comprises a first conductive layer for providing power and ground connections to driver electronics (page 9, paragraph 122, page 11, paragraph 139, Lines 11-14, paragraph 140, Lines 13-16).

Regarding Claim 13, Mathis et al. teaches an input/output (I/O) connector in communication with the connection layer configured for external communication (see figure 12, page 9, paragraphs 122).

4. Claims 4-8 and 10, are rejected under 35 U.S.C. 103(a) as being unpatentable over Matthies et al. (US 2005/0078104 A1) in view of Hayashi et al. (6,359,666 B1) and Fukuda, Masafumi (US 20020044142 A1) as applied to claims 1-3,12,13 above, and further in view of Salerno et al. (5,396,304).

Regarding Claim 4,5,6,7,8,10, Mathis et al. further teaches a large area display (page 1, paragraph 2, page 3, paragraph 75, page 4, paragraphs 75,76, 78, 80, page 8, paragraph 116,120, page 9, paragraph 121,122); the connection layer comprises a first conductive layer for providing power and ground connections to driver electronics (page 9, paragraph 122) and large area liquid crystal display (LCD, page 3, paragraph 70, Lines 5-11).

However, Mathis et al. modified by Hayashi et al. fails to recite and disclose the pixel layer comprises an active matrix display; the pixel layer comprises a passive matrix display; the pixel layer comprises at least one transistor per pixel; each of the at least one transistors comprises a thin film transistor (TFT); the drivers comprise complementary metal on semiconductor (CMOS) circuitry on silicon or glass substrates.

Salerno et al. teaches the pixel layer comprises an active matrix display (Col. 48, Lines 6-9); the pixel layer comprises a passive matrix display (Col. 48, Lines 9-12); the pixel layer comprises at least one transistor per pixel (Col. 15, Lines 31,32); each of the at least one transistors comprises a thin film transistor (TFT) (Col. 44, Lines 31-33); the drivers comprise complementary metal on semiconductor (CMOS) circuitry on silicon or glass substrates (Col. 44, Lines 60-68, Col. 2, lines 5-20); the drivers further comprise: serial data input for receiving display data; and serial data output for sensing and testing for light intensity transmitted through each light valve (Col. 35, Lines 49-65).

The reason to combine teaching of Salerno et al. with teaching of Matthis et al. teaching of large area LCD to overcome problem of amorphous silicon TFT's lack of needed frequency response in the large area high resolution LCD display technology.

Thus it is obvious to one in the ordinary skill in the art at the time of invention was made to incorporate teaching Salerno et al. of in teaching of Mathis et al. modified by Hayashi et al. and Fukuda, Masafumi to able to have a large area display with active matrix or passive matrix organization, as well as TFT driver for pixels with CMOS low power technology to produce highly defined color images.

5. Claim 9 is rejected under 35 U.S.C. 103(a) as being unpatentable over Matthies et al. (US 2005/0078104 A1) in view of Hayashi et al. (6,359,666 B1) and Fukuda, Masafumi (US 20020044142 A1) as applied to claims 1-3,12,13 above, and further in view of Yoshii et al. (6,147,724).

Regarding Claim 9, Matthis et al. further teaches a large area display (page 1, paragraph 2, page 3, paragraph 75, page 4, paragraphs 75,76, 78, 80, page 8, paragraph 116,120, page 9, paragraph 121,122); the connection layer comprises a first conductive layer for providing power and ground connections to driver electronics (page 9, paragraph 122) and large area LCD; liquid crystal display (page 3, paragraph 70, Lines 5-11).

However, Mathis et al. modified by Hayashi et al. fails to recite and disclose low voltage differential signaling (LVDS) logic for data transmission.

Yoshii et al. teaches the low voltage differential signaling (LVDS) logic for data transmission (Col. 25, Lines 20-52) and large area portable LCD; liquid crystal display (Col. 8, Lines 31-36).

The reason to combine teaching of Yoshii et al. with teaching of Matthis et al. teaching of large area LCD to reduce EMI, better ESD tolerance and noise tolerance for high speed serial data transfer in the large area high resolution LCD display technology.

Thus it is obvious to one in the ordinary skill in the art at the time of invention was made to incorporate teaching Yoshii et al. of in teaching of Mathis et al. modified by Hayashi et al. and Fukuda, Masafumi to able to have a highly defined color images large area display with active

matrix or passive matrix organization, as well as TFT driver for pixels with LVDS technology serially receiving high speed data with reduce EMI, better ESD tolerance and noise tolerance.

6. Claim 11 is rejected under 35 U.S.C. 103(a) as being unpatentable over Matthies et al. (US 2005/0078104 A1) in view of Hayashi et al. (6,359,666 B1) and Fukuda, Masafumi (US 20020044142 A1) as applied to claims 1-3,12,13 above, and further in view of Albert et al. (US 2005/0007336 A1).

Regarding Claim 11, Mathis et al. teaches a large area display (page 1, paragraph 2, page 3, paragraph 75, page 4, paragraphs 75,76, 78, 80, page 8, paragraph 116,120, page 9, paragraph 121,122); the connection layer comprises a first conductive layer for providing power and ground connections to driver electronics (page 9, paragraph 122) and large area bi-stable (electrophoretic) display (page 3, paragraph 70, Lines 5-11).

However, Mathis et al. modified by Hayashi et al. fails to recite and disclose the drivers comprise complementary metal on semiconductor (CMOS) circuitry on plastic substrates.

Albert et al. teaches the drivers comprise complementary metal on semiconductor (CMOS) (page 10, paragraph 102, Lines 1-4) circuitry on plastic substrates (page 4, paragraph 43, Lines 6-11) for a large area bi-stable (electrophoretic) display (page 9, paragraph 93, Lines 1-4).

The reason to combine teaching of Albert et al. with Mathis et al. teaching of bi-stable (electrophoretic) display to be able to bend or roll a portable large area display.

Thus it is obvious to one in the ordinary skill in the art at the time of invention was made to incorporate teaching Salerno et al. of in teaching of Mathis et al. modified by Hayashi et al. and Fukuda, Masafumi to able to have a large area display with organized, on plastic substrate with CMOS low power driver technology to produce a flexible large area display.

Response to Arguments

7. Applicant's arguments, see remark, filed on 02-12-2007, with respect to the amendments to claim1 have been fully considered and are persuasive. However, upon further consideration, a new ground(s) of rejection is made in view of Fukuda, Masafumi (US 20020044142 A1).

Conclusion

8. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure.

Odake; Ryota et al. (US 6426595 B1) Flat display apparatus.

9. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Prabodh M. Dharia whose telephone number is 571-272-7668. The examiner can normally be reached on M-F 8AM to 5PM.

10. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

11. Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

Any response to this action should be mailed to:

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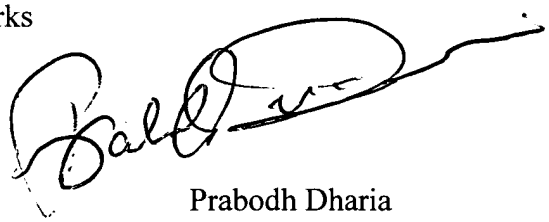

Prabodh Dharia

Partial Signatory Authority

AU 2629

March 20, 2007